IN THE CLAIMS

Please enter the following amendments to the claims. The amendments are believed to introduce no new matter.

1. (currently amended) A processor, comprising:

a plurality of registers;

processing circuitry associated with the plurality of registers, wherein the processing circuitry is operable to execute instructions included in a supported instruction set;

an instruction cache coupled to the processing circuitry, wherein the instruction cache is configured to provide copies of instructions in memory to the processing circuitry, the instruction cache including a first subset of instruction cache lines and a second subset of instruction cache lines, the second subset of instruction cache lines including one or more cache lines not included in the first subset;

wherein a the first subset of instruction cache lines ~~are~~ is invalidated using reset address line invalidate circuitry upon reset without using bypass circuitry, the first subset of instruction cache lines corresponding to instructions in memory used to invalidate the second subset of instruction cache lines.

2. (original) The processor of claim 1, wherein reset address line invalidate circuitry invalidates a single line in instruction cache upon reset.

3. (original) The processor of claim 1, wherein each line in the instruction cache comprises a tag portion and an instruction portion.

4. Cancelled

5. Cancelled

6. (currently amended) The processor of claim ~~5~~ 3, wherein the tag portion includes the state of an instruction cache line.

7. (currently amended) The processor of claim ~~5~~ 3, wherein the processor further comprises a data cache.

8. (previously presented) The processor of claim 7, wherein instructions copied comprise instructions for invalidating the second subset of instruction cache lines.

9. (original) The processor of claim 7, wherein instructions copied comprise instructions for invalidating all lines in the data cache.

10. (original) The processor of claim 1, wherein the processor is a processor core on a programmable chip.

11. (original) The processor of claim 10, wherein the processor is coupled to memory through a simultaneous multiple primary component fabric.

12. (previously presented) The processor of claim 10, wherein the processor can have its instruction cache invalidated and its data cache invalidated upon reset without the use of bypass circuitry.

13. (original) A programmable chip system, comprising:

processing circuitry associated with a plurality of registers, wherein the processing circuitry is operable to execute instructions included in a supported instruction set, the processing circuitry associated with reset address line invalidate circuitry operable to invalidate a first subset of cache lines upon reset without bypass circuitry, the first subset of cache lines corresponding to instructions in memory used to invalidate a second subset of cache lines, the second subset of instruction cache lines including one or more cache lines not included in the first subset;

a plurality of components coupled to the processing circuitry through an interconnection module.

14. (original) The programmable chip system of claim 13, wherein reset address line invalidate circuitry invalidates a single line in instruction cache upon reset.

15. (original) The programmable chip system of claim 13, wherein each line in the instruction cache comprises a tag portion and an instruction portion.

16. (previously presented) The programmable chip system of claim 15, wherein invalidating the first subset of instruction cache lines associated with the instruction cache comprises setting the tag portion of the first subset of instruction cache lines to invalid.

17. (previously presented) The programmable chip system of claim 16, wherein instructions from memory are copied into the instruction cache at the reset address line upon identifying that the first subset of instruction cache lines have been invalidated.

18. (original) The programmable chip system of claim 17, wherein the tag portion includes the state of an instruction cache line.

19. (original) The programmable chip system of claim 17, wherein the programmable chip system further comprises a data cache.

20. (previously presented) The programmable chip system of claim 19, wherein instructions copied comprise instructions for invalidating the second subset of cache lines.

21. (original) The programmable chip system of claim 19, wherein instructions copied comprise instructions for invalidating all lines in the data cache.

22. (original) The programmable chip system of claim 13, wherein the interconnection module is a simultaneous multiple primary component fabric.

23. (original) The programmable chip system of claim 22, wherein the processor can have its instruction cache invalidated upon reset without the use of bypass circuitry.

24. (previously presented) A method for performing a reset, the method comprising:

identifying a reset event at a processor;

invalidating a first subset of cache lines associated with processor cache without the use of bypass circuitry upon identifying the reset event, the first subset of cache lines corresponding to a plurality of instructions in memory used to invalidate a second subset of cache lines, the second subset of instruction cache lines including one or more cache lines not included in the first subset;

obtaining the plurality of instructions from memory, the plurality of instructions obtained after a read access request for the first subset of cache lines;

executing the plurality of instructions to invalidate a plurality of lines associated with the processor cache.

25. (currently amended) The method of claim 24, wherein the first subset of cache lines ~~are~~ is associated with a processor instruction cache.

26. (previously presented) The method of claim 24, wherein the plurality of instructions invalidates substantially all of the lines associated with processor cache.

27. (original) The method of claim 1, wherein reset events are associated with hardware faults and software faults.

28. (previously presented)A processor, comprising:

means for identifying a reset event;

means for invalidating a first subset of cache lines associated with processor cache without the use of bypass circuitry upon identifying the reset event, the first subset of cache lines corresponding to a plurality of instructions in memory used to invalidate a second subset of cache lines, the second subset of instruction cache lines including one or more cache lines not included in the first subset;

means for obtaining the plurality of instructions from memory, the plurality of instructions obtained after a read access request for the first subset of cache lines;

means for executing the plurality of instructions to invalidate a plurality of lines associated with the processor cache.